WHAT IS CLAIMED IS:

1. An inverter apparatus for driving a plurality of lamp units, each lamp unit including at least one lamp, the apparatus comprising:

a plurality of inverters, each inverter including a delay block delaying an input ON/OFF signal to generate an output ON/OFF signal and an inverting block controlling the lighting of the corresponding lamp unit based on the output ON/OFF signal,

wherein the plurality of inverters comprise a first inverter receiving the input ON/OFF signal from an external device and a second inverter receiving the input ON/OFF signal from one of the plurality of inverters.

2. The apparatus of claim 1, wherein the inverters are connected in series.

3. The apparatus of claim 1, wherein the first inverter is located at an outer side.

4. The apparatus of claim 1, wherein the delay block comprises:

a capacitor;

a first switch controlled by the input ON/OFF signal and providing a charging path for the capacitor upon activation;

a resistor connected to the capacitor and providing a discharging path for the capacitor; and

a second switch controlled by a voltage charged in the capacitor, providing a first voltage as the output ON/OFF signal upon inactivation, and providing a second voltage as the output ON/OFF signal upon activation.

5. The apparatus of claim 4, wherein the first switch outputs the first voltage as the charging path upon activation.

6. The apparatus of claim 4, wherein the resistor provides the second voltage as the discharging path.

7. The apparatus of claim 4, wherein a resistance of the resistor is determined such that time constant for the charging path is different from time constant for the discharging path.

8. The apparatus of claim 7, wherein the time constant for the charging path is smaller than the time constant for the discharging path.

9. The apparatus of claim 4, wherein the second switch is activated when the voltage charged in the capacitor is larger than a predetermined value and is inactivated when the voltage charged in the capacitor is smaller than the predetermined value, and the first voltage is larger than the second voltage.

10. The apparatus of claim 9, wherein a resistance of the resistor is determined such that a charging time of the capacitor is smaller than a discharging time for the capacitor.

11. The apparatus of claim 4, wherein the second voltage is a ground voltage.

12. The apparatus of claim 4, wherein the first switch comprises a pnp transistor and the second switch comprises an npn transistor.

13. The apparatus of claim 4, wherein the first voltage has substantially the same value as a high level of the input ON/OFF signal of the first inverter and the second voltage has substantially the same value as a low level of the input ON/OFF signal of the first inverter.

14. An inverter apparatus for driving a plurality of lamp units including first and second lamp units, each lamp unit including at least one lamp, the apparatus comprising:

a delay block receiving an input ON/OFF signal and stepwise delaying the input ON/OFF signal to generate a plurality of output ON/OFF signals; and

a plurality of inverters controlling the lighting of the respective lamp units based on the respective output ON/OFF signals.

15. The apparatus of claim 14, wherein the delay block comprises a plurality of RC circuits connected in series and one of the RC circuits receives the input ON/OFF signal.

16. A liquid crystal display comprising:

a panel assembly including a plurality of pixels, a plurality of gate lines connected to the pixels, and a plurality of data lines connected to the pixels;

a plurality of lamp units for illuminating the panel assembly;

a gate driver for providing signals for the gate lines;

a data driver for providing signals for the data lines;

a controller for providing image signals for the data driver and control signals for the gate driver and the data driver and generating an ON/OFF signal for driving the lamp units;

a delay block delaying the ON/OFF signal from the controller; and

an inverting block controlling the lighting of one of the lamp units based on the delayed ON/OFF signal.

17. The liquid crystal display of claim 16, wherein the delay block comprises:

a capacitor;

a first transistor controlled by the ON/OFF signal and providing a charging path for the capacitor upon activation;

a resistor connected to the capacitor and providing a discharging path for the capacitor; and

a second transistor controlled by a voltage charged in the capacitor, providing a first voltage as the delayed ON/OFF signal upon inactivation, and providing a second voltage as the delayed ON/OFF signal upon activation.

18. The liquid crystal display of claim 17, wherein a resistance of the resistor is determined such that time constant for the charging path is different from time constant for the discharging path.

19. The liquid crystal display of claim 17, wherein the second transistor is activated when the voltage charged in the capacitor is larger than a predetermined value and is inactivated when the voltage charged in the capacitor is smaller than the predetermined value, the first voltage is larger than the second voltage, and a resistance of the resistor is determined such that a charging time of the capacitor is smaller than a discharging time for the capacitor.

20. The liquid crystal display of claim 16, wherein the delay block comprises an RC circuit.